CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a substrate;

at least one inter-level dielectric (ILD) layer having a low dielectric constant (k); and

at least one support structure disposed in the ILD layer to mitigate damage of the semiconductor device caused by stresses to the ILD layer.

2. The semiconductor device of claim 1, wherein the at least one ILD layer has an ultra low dielectric constant (k).

3. The semiconductor device of claim 1, wherein the at least one support structure is one of a trench and via formed from a support material.

4. The semiconductor device of claim 3, wherein the support material comprises at least one of aluminum, aluminum alloy, copper, copper alloy, tungsten, or tungsten alloy.

5. The semiconductor device of claim 1, wherein the support structure mitigates damage of the ILD layer due to forces applied onto the ILD layer during one of a subsequent processing and packaging of the semiconductor device.

6. The semiconductor device of claim 1, further comprising:

a plurality of low-k ILD layers, and

at least one support structure disposed in each of the plurality of low-k ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to form a support column.

7. The semiconductor device of claim 6, wherein the support structures are located underneath the source of the stress to mitigate damage to the semiconductor device.

8. The semiconductor device of claim 7, the source of the stress being a bond pad location.

9. The semiconductor device of claim 6, further comprising at least one additional ILD layer having a dielectric constant which is higher than the low-k ILD layer overlying the at least one low-k inter-level dielectric layer.

10. The semiconductor device of claim 9, the support column ending at the at least one additional ILD layer

11. The semiconductor device of claim 9, further comprising at least one support structure disposed in the at least one additional ILD layer.

12. The semiconductor device of claim 1, wherein a plurality of support structures are disposed in the at least one low-k dielectric layer in an n x m matrix configuration, where n and m are integers greater than one.

13. The semiconductor device of claim 12, wherein a plurality of support structures are disposed in the at least one low-k dielectric layer at a plurality of locations spaced equidistant apart from each other across substantially the entire layer.

14. The semiconductor device of claim 12, wherein the plurality of support structures are disposed at a location below a bond pad disposed on the semiconductor device.

15. A method of forming a semiconductor device comprising:
providing a substrate;
forming a low-k inter-level dielectric (ILD) layer over the substrate;
forming at least one opening in the low-k ILD layer; and
filling the at least one opening with a support material to form a support structure in the low-k ILD layer, the support structure mitigating damage to the semiconductor device caused by stresses to the low-k ILD layer.

16. The method of claim 15, the at least one opening is one of a via and a trench.

17. The method of claim 15, further comprising forming a conductive layer over the low-k ILD layer, the filling of the at least one opening being formed during the formation of the conductive layer over the low-k ILD layer.

18. The method of claim 17, further comprising:
forming an additional ILD layer over the conductive layer;
forming a protective top layer over the semiconductor device; and
forming at least one bond pad disposed in the protective top layer at a location overlying the at least one support structure, the bond pad including a surface for receiving a solder bump.

19. The method of claim 18, further comprising forming at least one support structure disposed in the additional ILD layer.

20. The method of claim 19, the additional ILD layer having a dielectric constant which is higher than the low-k ILD layer.

21. The method of claim 15, the filling the at least one opening with a support material comprising filling the at least one opening with one of aluminum, aluminum alloy, copper, copper alloy, tungsten, tungsten alloy.

22. A method of reinforcing a semiconductor device to mitigate damage of the semiconductor device during one of processing or packaging:

providing a substrate;

forming an inter-level dielectric (ILD) layer over the substrate, the ILD layer being formed from a dielectric material having a dielectric constant (k) in the range of about 1.0 to about 3.8; and

forming a support structure filled with support material in the ILD layer, the support structure being formed in a location underneath a source of stress applied to the semiconductor during one of processing or packaging.

23. The method of claim 22, the dielectric material having a dielectric constant (k) in the range of about 1.0 to about 2.7.